

FORM PTO-892 (REV. 2-92)				U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		SERIAL NO. <u>07/852,517</u>	GROUP ART UNIT <u>2508</u>	ATTACHMENT TO PAPER NUMBER	<u>7</u>
NOTICE OF REFERENCES CITED				APPLICANT(S) <u>YAMAZAKI et al.</u>					

## U.S. PATENT DOCUMENTS

*	DOCUMENT NO.			DATE	NAME		CLASS	SUB-CLASS	FILING DATE IF APPROPRIATE
A	4	7	2	7	0	4	4	257	52
B	4	8	0	3	5	2	8	257	912
C	4	8	1	4	2	9	2	437	233
D	5	0	3	6	3	7	3	257	86
E	5	1	0	8	8	4	3	428	446
F									
G									
H									
I									
J									
K									

## FOREIGN PATENT DOCUMENTS

*	DOCUMENT NO.			DATE	COUNTRY	NAME	CLASS	SUB-CLASS	PERTINENT SHTS. DWG.	PP. SPEC.
L	57	10	26	7	1-82	JP	SAKURA I	257	66	
M	6	35	47	73	3-88	JP	HOSOKAWA	257	66	
N	1	28	64	63	11-89	JP	ISHIHARA	257	66	
O										
P										
Q										

## OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

R	<u>WOLF et al., "SILICON PROCESSING FOR THE VLSI ERA," VOL. 1, LATTICE PRESS, SUNSET BEACH, CALIFORNIA, PP. 19-21</u>								
S									
T									
U									

EXAMINER	<u>m. Saadat</u>	DATE	<u>3-5-93</u>
----------	------------------	------	---------------

\* A copy of this reference is not being furnished with this office action.  
(See Manual of Patent Examining Procedure, section 707.05 (a).)